REMARKS

This communication responds to the Office Action mailed on August 30, 2006. Claim 68 is amended (to correct a typographical error, and not for reasons related to patentability), no claims are canceled, and no claims are added. As a result, claims 36-39, 59-69, and 75-83 are now pending in this Application.

In the Specification

The specification has been amended to update the priority information of the related application. No new matter has been added.

Double Patenting Rejection

Claims 65-67 were rejected under the judicially created doctrine of obviousness-type double patenting over claims 1, 4, 7, 11, 12, and 15 of U.S. Patent No. 6,615,325 in view of Ogawa, U.S. Patent No. 5,293,347. The Applicant does not admit that the claims are obvious over U.S. Patent No. 6,615,325 in view of Ogawa. However, a Terminal Disclaimer in compliance with 37 CFR 1.321(b)(iv) is enclosed herewith to obviate this rejection, since the Office has indicated the claims are otherwise in condition for allowance.

§103 Rejection of the Claims

Claims 59-62 and 68-69 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Manning (U.S. 5,610,864) in view of Roy (U.S. 6,065,092) or Ogawa (U.S. 5,293,347). First, the Applicant does not admit that Manning, Ogawa, or Roy are prior art, and reserves the right to swear behind these references in the future. Second, because no *prima facie* case of obviousness has been established, the Applicant respectfully traverses this rejection.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). The M.P.E.P. contains explicit direction to the Examiner in accordance with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in

> the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

No proper *prima facie* case of obviousness has been established because (1) combining the references does not teach all of the limitations set forth in the claims, (2) there is no motivation to combine the references, and (3) combining the references provides no reasonable expectation of success. Each of these points will be explained in detail, as follows.

The Combination of References Does not Teach All Limitations: As stated by the Board of Patent Appeals and interferences (BPAI), "Manning provides no details as to how the use of a pipelined structure might be accomplished. We agree with appellants. Manning's suggestion to use a pipeline architecture is insufficient to suggest switching between burst and pipelined modes. As indicated supra, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur. Accordingly, we cannot sustain the obviousness rejection ...". BPAI, Appeal No. 2005-1725, March. 20, 2006. Thus, Manning fails to teach switching between burst and pipelined modes. This is also the case with Roy and Ogawa.

Roy describes a memory device capable of column burst activity where sequential bytes of data are accessed using a starting column and row address and a burst length. *See* Roy, Col. 26, lines 62-66. New actions may be initiated when a burst is completed. *See Id.* at Col. 27, lines 4-14. The device may also be used in a pseudo-pipelined access mode, such that a new column address is provided every cycle for a random read operation, as long as it is confined to a selected row. *See Id.* at Col. 28, lines 16-32 and Col. 33, lines 8-19. While limited access

pseudo-pipelined reads may occur once per cycle, pseudo-pipelined write operations occur at only one-half the maximum channel frequency, since channel access is shared by both addresses and data. *See Id.* at Col. 33, lines 65-67. This is in direct contrast to the teachings of the Applicant, which enable true pipelined operation, with column-based switching in addition to row-based switching (See Application, pg. 38, lines 7-16). The Applicant was unable to find any indication that Roy enables selecting true pipelined and burst operation "on the fly" as demonstrated by the Applicant's disclosed embodiments (due to restriction imposed by software header mode changes and channel data/address sharing). For example, Roy does not permit row-based switching operation (i.e., "... cannot be used to change a row in every cycle ..."). *Id.* at Col. 38, lines 23-24.

While claims during examination should be interpreted as broadly as their terms reasonably allow, that interpretation must be tempered by the context in which the terms are used. The *Hyatt* court states that "during examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 U.S.P.Q.2D (BNA) 1664, 1667 (Fed. Cir. 2000) (emphasis added) ("During examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification."; citing *In re Graves*, 69 F.3d 1147, 1152, 36 U.S.P.Q.2D (BNA) 1697, 1701 (Fed. Cir. 1995); *In re Etter*, 756 F.2d 852, 858, 225 U.S.P.Q. (BNA) 1, 5 (Fed. Cir. 1985) (en banc).).

The interpretation of the term "pipelined mode" proffered by the Office with respect to Roy is neither reasonable, nor consistent with the specification. It is not reasonable because it contradicts the meaning of the term as understood by those of skill in the art. The interpretation by the Office is also not consistent with the specification. Thus, any attempt by the Office to characterize Roy as teaching a true "pipelined mode" of operation is beyond that which should be reasonably allowed, and the rejection of claims under 35 U.S.C. § 103(a) is improper.

Ogawa presents similar difficulties, since pipelined access is described only with respect to a single mode of operation – the page mode. *See* Ogawa, Abstract and Col. 1, lines 8-12. "The page mode processing is an operation that subsequently reads out data in memory cells connected to one word line selected by a row address by sequentially changing the column

address ...". Col. 4, lines 4-8. While Ogawa notes that "the present invention is not limited to the page mode, and the concept of the present invention can be similarly applied to random read/write operation" at Col. Col. 12, lines 5-10, this statement of potential use with respect to random read/write operations does not lead one of ordinary skill to understand how switching between burst and pipelined modes would be accomplished, since Ogawa does not teach any kind of switching behavior. As is the case with Roy, Ogawa provides no indication of how memory access operations can be conducted in conjunction with switching between burst an pipelined modes "on the fly" as taught by the Applicant.

Finally, as noted by the BPAI, "Manning's suggestion to use a pipelined structure is insufficient to suggest switching between burst and pipelined modes. As indicated **supra**, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur." BPAI, Appeal No. 2005-1725, March. 20, 2006. The Applicant also finds nothing in Manning to suggest substituting a pipelined mode for the page mode, as suggested by the Office with respect to Ogawa. Therefore, no combination of Manning and either Roy or Ogawa can provide "choosing whether the memory is in a burst mode of operation or a pipelined mode of operation" or "selecting a burst or a pipeline mode of operation", much less "mode circuitry configured to select between a burst mode and a pipelined mode" as claimed by the Applicant.

No Motivation to Combine the References: The Office asserts that "it would be obvious ... to include the memory selectively operable in a pipeline mode of Roy in the invention not Manning because it would increase memory performance of Manning by providing a new column address every cycle ..." However, this suggestion to combine the references overlooks the fact that neither Manning nor Roy teach switching between a pipelined mode and another mode. Neither does Ogawa.

In addition, this assertion overlooks the limitations of Roy's pseudo-pipelined access, namely: (1) read operations are confined to the same row (no row-based switching), and (2) write operations only occur at one-half the channel speed; not at the full speed of the channel.

Finally, combining Roy with Manning also overlooks the following statement in Manning: "An integrated circuit memory device is designed for high speed data access and

compatibility with *existing* memory systems." (Manning, Abstract, emphasis added). The device is made to be compatible with existing systems; not radically new systems, such as that described by Roy, in which "[o]ne of the fundamental features of this architecture is the use of the same lines of a data channel for both address and control information, as well as for bi-directional data transfers. Data read and write operations within the memory device are organized into discrete "transactions," with each such transaction initiated by several sequential data words termed a "header." The header includes address and control information for a subsequent transfer of one or more bytes of data into or out of the memory device. The header can be applied to one channel for a subsequent transaction across that same channel or across another channel." *Roy*, Col. 9, lines 12-22. Thus, Manning teaches away from the asserted combination, since the two devices are fundamentally incompatible. Therefore, since there is no evidence in the record to support this assertion, as required by the *In Re Sang Su Lee* court, it appears the Examiner is actually using personal knowledge, and the Examiner is respectfully requested to submit an affidavit supporting such knowledge as required by 37 C.F.R. § 1.104(d)(2).

It is respectfully noted that the test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *See Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985) (emphasis added). References must be considered in their entirety, including parts that teach away from the claims. See MPEP § 2141.02. Since Roy teaches away from using a true pipelined mode (as well as from being used in a conventional manner), and since Ogawa teaches away from any kind of mode switching during operation, there is no motivation to combine these references.

No Reasonable Expectation of Success: Roy teaches the use of a pseudo-pipelined mode. Ogawa teaches the use of a single mode of operation, without switching. Combining either of these references with Manning would not lead one of ordinary skill in the art to expect success, since the function of switching between burst and pipelined modes would not be enabled, nor would the design of circuitry configured to select between burst and pipelined modes of operation.

The use of unsupported assertions in the Office Action does not satisfy the explicit requirements needed to demonstrate motivation as set forth by the *In re Sang Su Lee* court. Therefore, the Examiner appears to be using personal knowledge, and is again respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

In summary, the references neither teach nor suggest selecting/choosing between burst and pipelined modes of operation, and the modifications suggested by the Office do not lead to a reasonable expectation of success by one of ordinary skill in the art. In fact, each of the references teach away from such a combination. Thus, the requirements of *M.P.E.P.* § 2142 have not been satisfied; and a *prima facie* case of obviousness has not been established with respect to the Applicant's claims. It is therefore respectfully requested that the rejection of claims 59-62 and 68-69 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Allowable Subject Matter

The Examiner has indicated that claims 36-39, 63-64, and 75-83 are allowable. As noted previously, claims 65-67 have been indicated to be allowable if the double patenting rejection tendered by the Office is overcome via terminal disclaimer.

CONCLUSION

The Applicant respectfully submits that all of the pending claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney (210) 308-5677 to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 30 day of October 2006.

KATE GANNON

Name

Signature